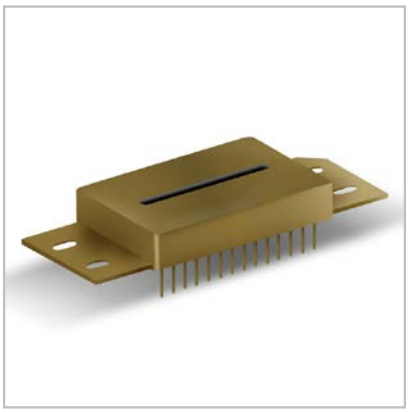
IG Series Linear Array Architecture

IG22/IG26-Series Standard Features

- 28 Pin Package with 256 Element InGaAs array
- AutoZero front end with input offset <100 µV
- Variable charge well $2x10^6$ to $230x10^6$ electrons in 256 steps
- Single 5 Volt power supply operation
- Built in reference voltage
- Low power design
- Clock rate 100 kHz – 1 MHz



Absolute Maximum Ratings

- VDD 6 V
- Any Pin VDD +0.5 V, VSS -0.5 V

03/17 / V02 / IF / lcdgi/ig-line-array-architecture

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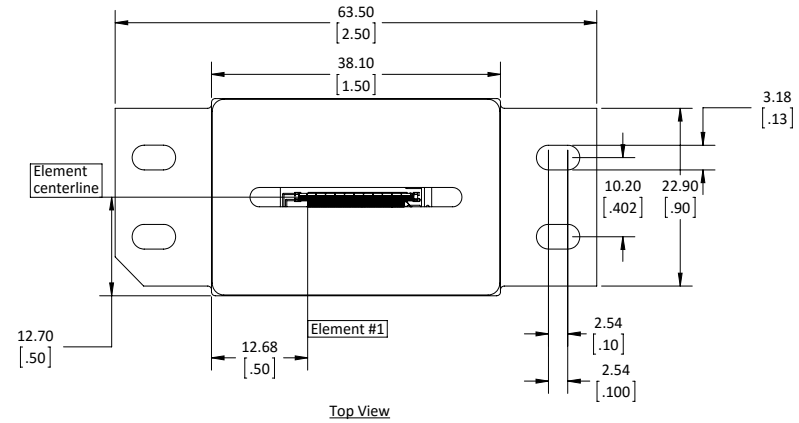
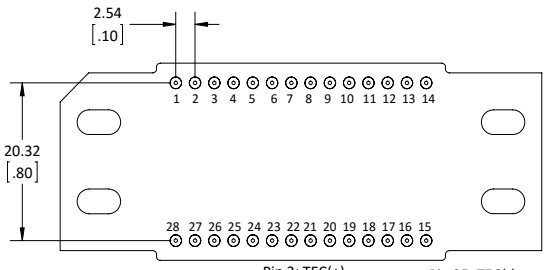
1. Drawing



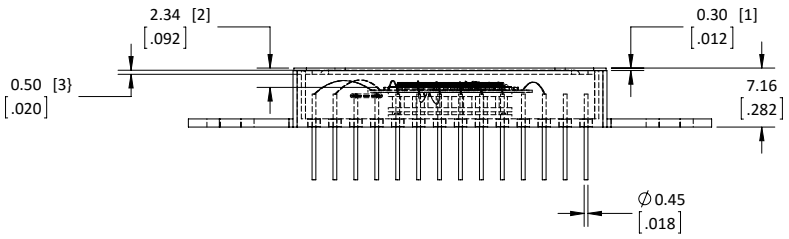
Top View



Bottom View

Pin 3: TEC(+)
Pin 4: TEC(+)
Pin 6: THERMISTOR
Pin 7: THERMISTOR
Pin 8: POST-OUT
Pin 9: PRE-OUT
Pin 10: SETWELL1
Pin 12: SETWELL2
Pin 20: ROCLOCK
Pin 22: GROUND
Pin 23: +5V
Pin 24: EOS

Pin 25: TEC(-)
Pin 26: TEC(-)
Pin 27: INTTIME
Pin 28: SETWELL0



Side View

[1] Distance from top of device to top of window.

[2] Distance from top of active area to top of device.

[3] Window thickness.

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2. Die Pad Control

Rather than using the digital control system built into the multiplexer, (which would require either a small micro or an FPGA to be able to load the serial registers on power up) the InGaAs array uses a simpler method of setting up the multiplexer. It was designed to use a simple bond pad method of configuring the majority of the multiplexer features by internal hard wiring. The only features not available through die pad control interface are per channel gain, and windowing.

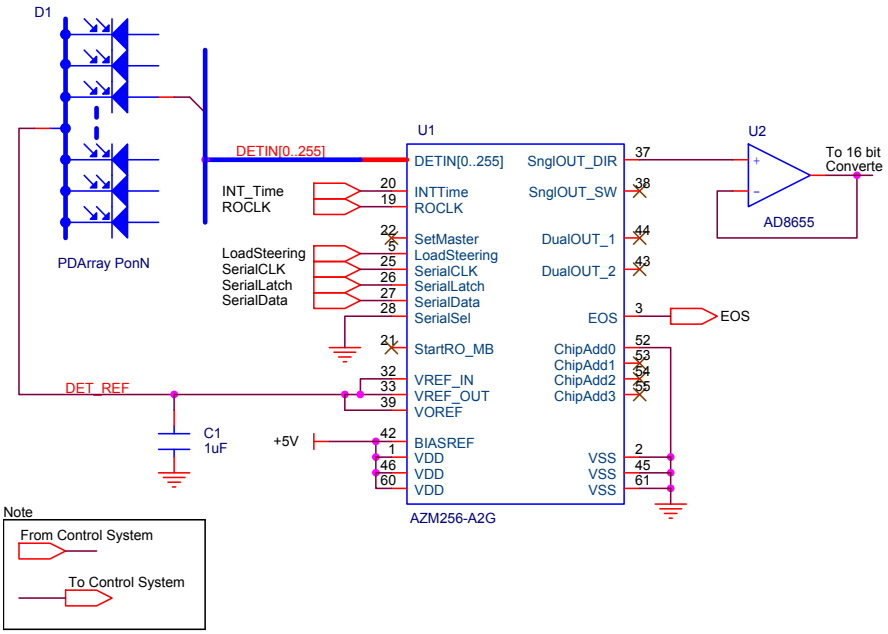

Figure 1: Single 256 Element ROIC with Die Pad Control Implementation

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In the standard IG arrays, the following interfaces are available to the user:

Table 1: 28 pin package control and data interfaces

I/O	Package Pin Position	Type
INTTime	27	CLKI
ROCLK	20	CLKI
EOS	5	DO
Pre-Out	9	Analog O
Post-Out	8	Analog O
SetWell0	28	DI
SetWell1	10	DI
SetWell2	12	DI

The following die pads have been preconfigured:

Table 2: Preconfigured Die Pad Controls

Function	Configuration
SerialSel	Diepad Control
GlblGainMode	Global Gain (Only Option)
DisBRST	Disabled
SetRefOPAON	Preconfigured Internal Bias
FilterBW2	Preconfigured total resistance = 125K
FilterBW1	Included above
FilterBW0	Included above
SetModeA	Preconfigured Internal Timing
SetDualCDS	Preconfigured Single Stage
DisQSRST	Preconfigured Disabled
SetRODIR	Preconfigured Left-to-Right
Set256	Preconfigured for 256 Elements
SetSingle	Preconfigured for Two Differential Outputs
SetOutGain1	Set for Total Gain = 1
SetOutGain0	Included above

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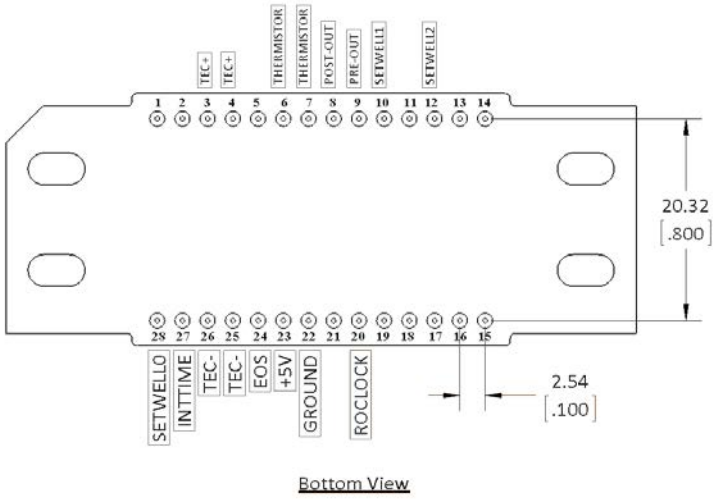

Figure 2: 28 Pin Package Connections

SetWell2, SetWell1, and SetWell0:

This system allows a selection of binary weighted charge well values from a minimum 125fF to the maximum of 16pF. The table below details the operation of the die pads.
Note that a "1" in the table signifies a logic HIGH place on the die bond pad. The default state is "1" due to the internal pull up circuit that is attached to every digital input.

Table 3: Setting Capacitor Well Size

SetWell2	SetWell1	SetWell0	Capacitance
0	0	0	125fF
0	0	1	250fF
0	1	0	500fF
0	1	1	1pF
1	0	0	2pF
1	0	1	4pF
1	1	0	8pF
1	1	1	16pF

A note about digital inputs.

All of the digital inputs into the multiplexer are TTL compatible and will function properly with operating voltages (VDD) anywhere from 4.5 Volts to 6 Volts. In addition, all of the digital inputs incorporate pull ups on their input, which provides a stable logic HIGH on the input should the pad be left unbonded.

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3.Timing:

Integration Timing:

Internal Timing Mode:

Internal timing mode is preset via the SetModeA die pad. In this timing mode all of the timing signals needed to operate the mux are generated from two input signals, the readout clock (ROCLK) and the integration clock (INTTime). In a clocked system such as this one, the timing of switch closings and openings is directly related to the pixel clock. An understanding of when events are occurring inside the multiplexer can be helpful when deciding on the proper timing of inputs. For the following discussion please refer to Figure 3, which shows a simplistic block diagram of a mux channel with all the major internal switches shown. The signal names used in the subsequent timing diagrams will be taken from Figure 3. Assume that all signal polarities are positive, meaning a logic HIGH on the control line of any of the switches in Figure 3 will close that particular switch.

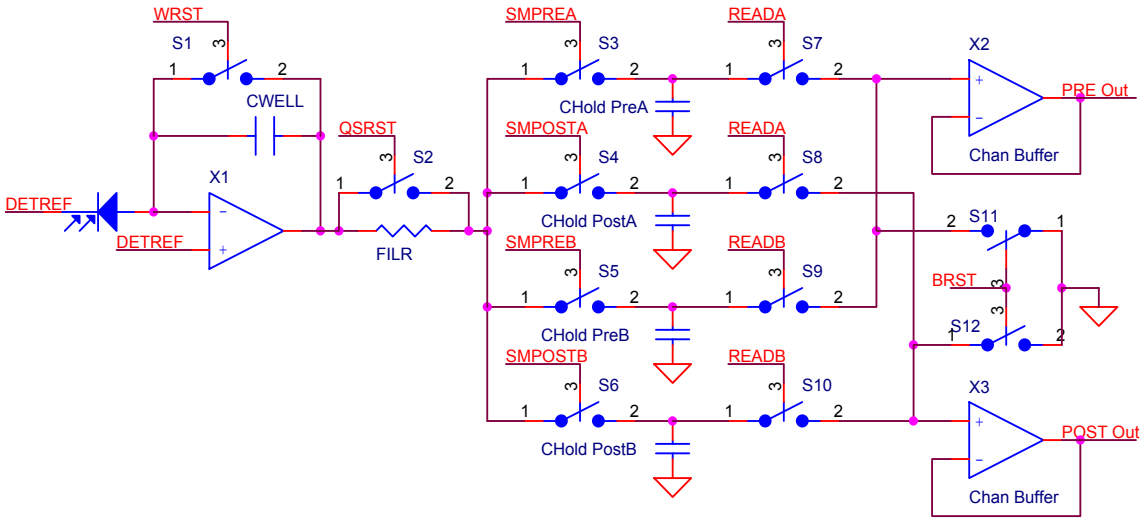

Figure 3: Integration timing block diagram

Single CDS: See Figures 4 and 5 for the start and end of integration timing diagrams for the internal timing mode with single CDS. The single CDS case is set by turning off the Dual CDS stage in the configuration. Without a dual stage CDS there cannot be an overlap of readout and integration. As can be seen in the timing diagrams (Figures 4 and 5) the sample pre and post B and the read B are always off and only the A bank is used.

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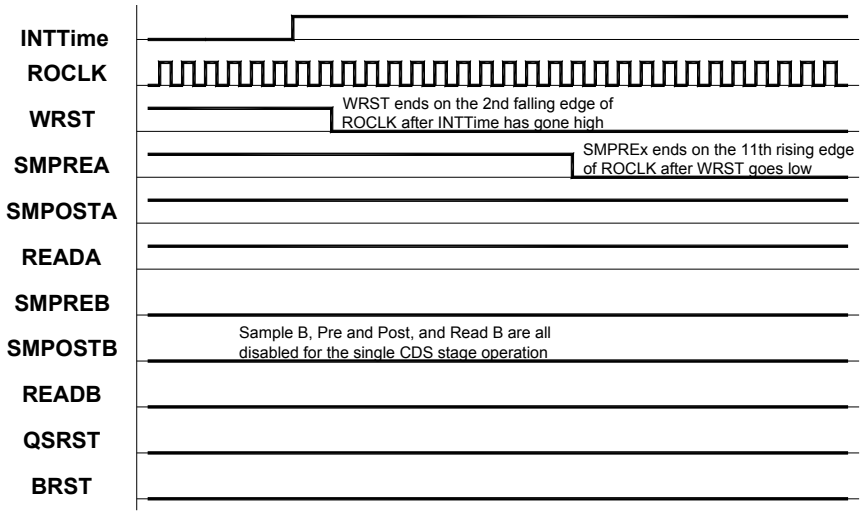

Figure 4: Start of integration for internal timing with a CDS stage.

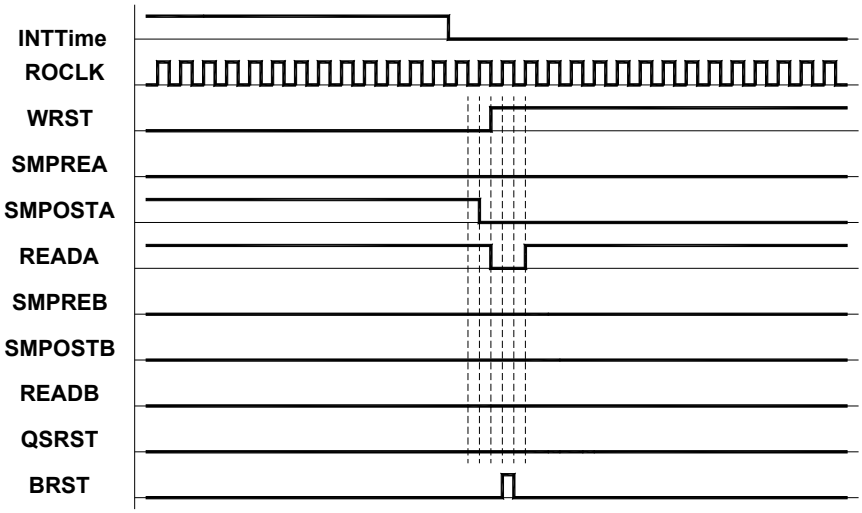

Figure 5: End of integration for the interal timing single CDS Case.

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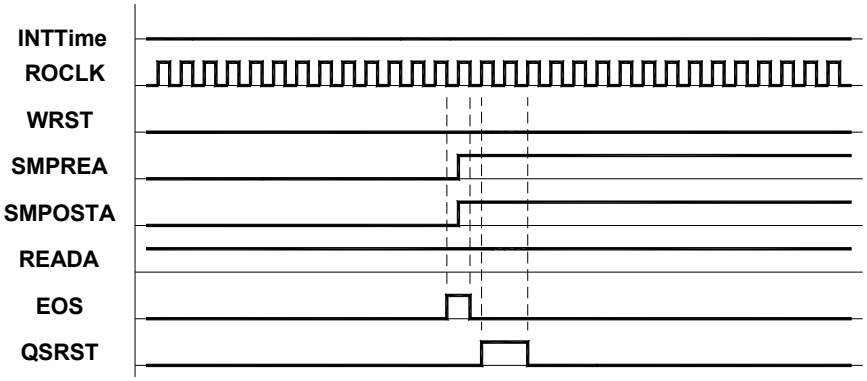

Figure 6: QSRST operation during single stage CDS internal timing

Figure 6 shows the action of the quick sample reset (QSRST) for the single CDS stage case (which is a feature that is not implemented). The EOS (end of scan) pulse represents the end of readout (see section on readout timing for details on EOS). At the end of readout the two samples, Pre and Post, turn on and then the QSRST turns on for two readout clock cycles. The QSRST operation whether it is used or not, does require some time from the end of readout (signified by EOS) till the next integration time for the single CDS timing case. That time is recommended to be 10 readout clock cycles.

Although the previous discussions of timing may seem complex, the actual timing supplied by the user is simple when using the internal timing generator, just an integration clock and a readout clock. This is the configuration that has been implemented and is summarized in Figure 7.

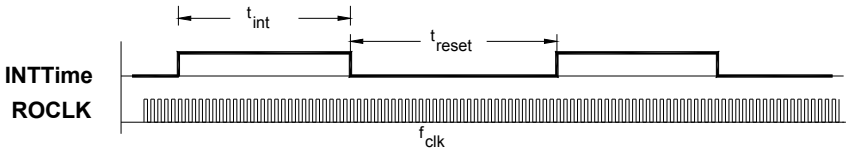

Figure 7: Required Inputs for Interal Timing Single CDS Operation

- Readout after integration operation.
- f_{clk} should be a continuous 50% duty cycle clock with a frequency of 100 kHz to1 MHz. Other frequencies are possible but may require adjustment to internal current sources or external timing.
- t_{int} must be a minimum of 13 ROCLK periods wide.
- Readout must be completed prior (10 clock cycles recommended) to the arrival of the next integration time.

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Readout Timing:

The critical knowledge needed when implementing any multiplexer based system, is to know when the first useful channel shows up at the analog output, and then at what rate to the remaining channels arrive at the same output. These questions are the core of what readout timing is all about.

Master / Slave Configuration: While the multiplexer has the capability to support the master/slave relationship of multiple units, the array has been preconfigured for master operation only. The selection is made by the bonding of Set Master die pad to a logic high (or left unbonded). For all applications which involve a single multiplexer die, the intention is that the ROIC will be in the Master mode. Slave mode is intended for multi multiplexer arrays, where it is necessary to chain the readout of the multiple ROICs one after the other. In a multi ROIC application the first mux in the readout chain would be a Master multiplexer, and it would be configured as a master timing mode device. All additional ROICs in the array would be configured as slaves.

Internal Timing Mode:

Start of Readout - Master Mode: The internal timing approach to readout is very simple, it is based on a fixed timing relationship between the integration clock (INTTime) and the readout clock (ROCLK). The first pixel always arrives at the same time – which is on the 6th rising edge of ROCLK following a falling edge of integration clock (INTTime).

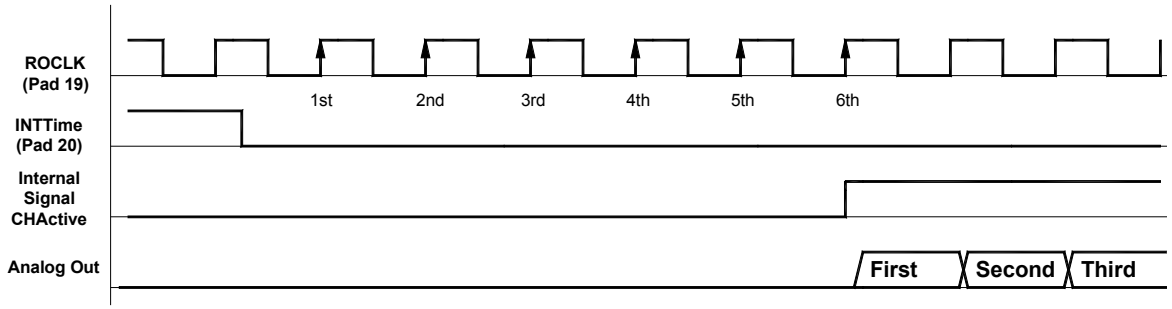

Figure 8: Readout Timing - Internal Master Mode

The CHActive line shown in figure 8 is an internal timing signal that is generated from the user inputs. Its sole purpose is to control the switch that is between the output of the internal difference amplifier and- the DiffOut_ Switched output. This signal connects the output amplifier to the die pad ONLY when the ROIC is actively reading out channels. This allows the die pad 38's of multiple multiplexers to be connected directly together, greatly simplifying multiple ROIC array designs.

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End of Readout: The end of readout occurs when the last selected channel is readout on the analog port (see Figure 9). As a marker of this point in time, a digital output, **EOS**) is supplied by the ROIC. The EOS (End Of Scan) output has two functions, the first is to alert the system controller that the last channel has been read. The second is to provide a suitable signal for cascading the readout of multiple multiplexers, a feature that is not implemented on this array.

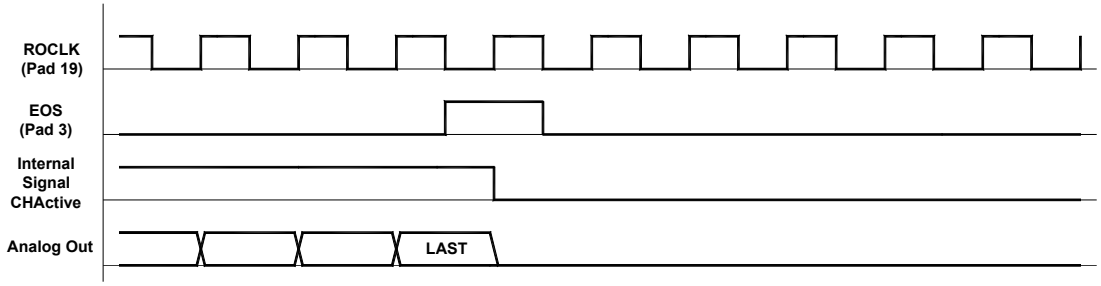

Figure 9: End of Readout Timing

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4. APPENDIX A: List of Die Pad Functions

SetModeA: When the die pad is a logic HIGH (or unbonded) the internal timing generator is selected. When the die pad is bonded to a logic LOW then the external timing mode is selected.

GlbGainMode: When the die pad is a logic HIGH (or unbonded) the multiplexer is in the global gain mode and all channels will have the same charge well size, controlled by the charge well size bond pads. If the GlblGainMode pad is bonded to a Logic LOW then the multiplexer will be in a per channel gain mode - which is not useable in a die pad configuration mode. Therefore, this pad is always unbonded when using the die pad configuration control method.

DisBRST: When this die pad is a logic HIGH (or unbonded) the buss reset timing signal is disabled. When the die pad is bonded to a logic LOW then the buss reset is enabled and can come from either the internal timing generator or from the external timing input pad ExtBRST.

SetRefOPAON: When the die pad is a logic HIGH (or unbonded) the internal voltage reference opamp is powered. When the die pad is bonded to a logic LOW then the voltage reference opamp is off and an external bias must be used for driving the detector substrate.

FilterBW2, 1, and 0: Using the following table (table A1) the operation of these die pads can be determined. For example, when all three die pads are a logic HIGH (or left unbonded) then the selected filter resistance is 125K ohms - and when all three die pads are bonded to a logic LOW, the selected resistance is 1 megohm.

Table A1: Filter resistance

B2	B1	B0	Resistance
1	1	1	125K
1	0	1	375K
1	0	0	500K
1	1	1	625K
0	1	0	750K
0	0	1	875K
0	0	0	1000M

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Differential Outputs: There is an advantage in connecting a differential amplifier to the output channels of the multiplexer; noise performance can be improved. The circuit in figure A1shows an example of how to interface to the dual output option of the multiplexer. What is shown is a three amplifier difference amplifier attached to the two differential outputs. Depending on parts choice and bandwidth / noise requirements, this could be done with a single IC package, or it may be possible to find a differential input A/D that the mux can drive directly. Take care to not load the outputs of the multiplexer too heavily when attaching external circuitry. The capacitance of the load placed on any output will directly affect its slew rate and bandwidth. Any real impedance placed on the outputs will lower the open loop gain of the on board output amplifiers and result in reduced performance and increased power dissipation. As a rule keep real loads to 5Kohms or greater, and keeping the capacitance to less than 50pf, 30pf is preferred.

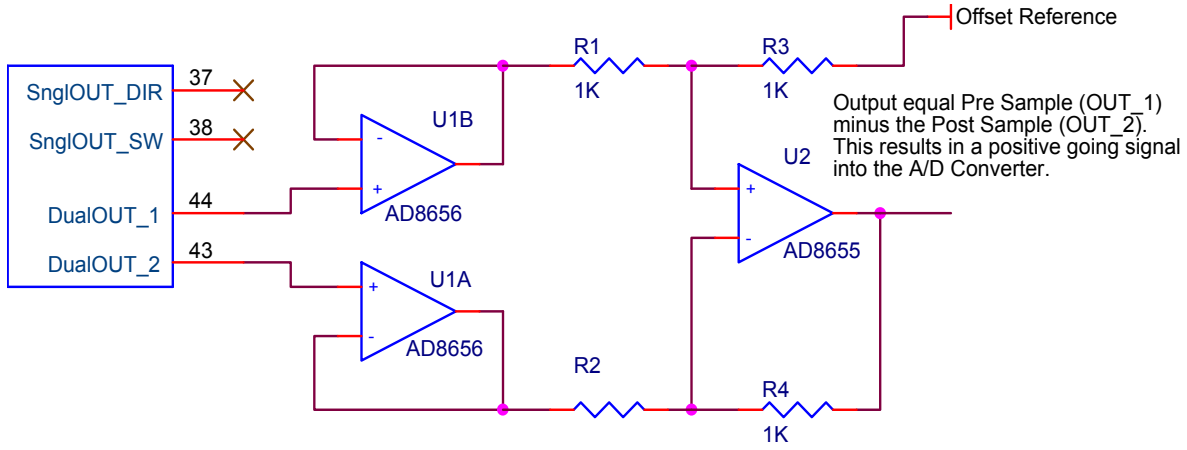

Figure A1: Differential Output Option Schematic

One further note, though not shown on any of the application schematics, it is always a good idea to have a noise bandwidth limiting filter (a real pole will do) on the input of the A/D converter, this eliminates any excess noise arising from the wideband nature of the output amps of the ROIC and the amps of the external circuitry.

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SetDualCDS: When the die pad is a logic HIGH (or unbonded) the dual stage CDS system is engaged. When the die pad is bonded to a logic LOW then CDS is reduced to a single stage.

DisQSRST: When the die pad is a logic HIGH (or unbonded) the quick sample reset timing signal is disabled. When the die pad is bonded to a logic LOW then the quick sample reset is enabled and can come from either the internal timing generator or from the external timing input pad **ExtQSRST.**

SetRODIR: When the die pad is a logic HIGH (or unbonded) the multiplexer is read out from left to right. When the die pad is bonded to a logic LOW the multiplexer reads out right to left.

Set256: When the die pad is a logic HIGH (or unbonded) the multiplexer is configured as a 256 channel mux. When the die pad is bonded to a logic LOW the multiplexer is configured as a 128 channel mux.

SetSingle: When the die pad is a logic HIGH (or unbonded) the multiplexer uses its internal difference amplifier and the output is presented on two output die pads. When the die pad is bonded to a logic LOW the difference amp is turned off and the mux outputs the analog stream on the two differential output die pads.

SetOutGain0 and SetOutGain1: The operation of these gain bits is identical to that shown in table A2. Note that a "1" in the table signifies a logic HIGH place on the die bond pad. This is the same as the unbonded state due to the internal pull up circuit that is attached to every digital input.

Table A2: Amplifier Gain

Bit 1	Bit 0	Gain V/V
0	0	4
0	1	2
1	0	1.33
1	1	1

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